Article

An entangling gate for dual-rail erasure qubits

https://doi.org/10.1038/s41586-026-10822-y

Received: 6 May 2025

Accepted: 17 June 2026

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Quantum error correction (QEC) will likely be required to realize the full potential of quantum computing, but comes with daunting hardware overheads and demands low gate errors on the physical qubits[1–4]. These requirements can be eased by engineering qubits with a strong error hierarchy, in which the most common noise channels are also the easiest to correct. Erasure qubits can achieve this when detectable leakage errors out of the computational subspace dominate over the residual Pauli errors[5–11], resulting in higher thresholds and improved scaling with code distance[5,12,13]. In practice, these advantages come to fruition only if the error hierarchy is preserved as much as possible throughout all gates and operations. Here we design and realize a two-qubit entangling gate for dual-rail cavity qubits, a type of erasure qubit encoded in a pair of superconducting microwave cavities[7]. Our experimental demonstration confirms that the error hierarchy is largely preserved during the gate. The gate is fast (about 500 ns duration) and shows low erasure rates of approximately 0.5% per gate, remaining Pauli errors below 0.1%, and a strong bias towards dephasing errors, in which bit-flips are practically non-existent at the 10^{-6} level. These results enable a faster path to error-corrected systems that rapidly suppress errors as they scale; a claim we support with our detailed surface code simulations.

To progress from the present-day era of NISQ machines[14] to the era of effective quantum error correction (QEC), the performance of physical qubits and their fundamental operations must improve markedly. A useful approach to relax the requirements for QEC is to engineer qubits with structured noise, in which certain types of errors occur much more frequently than others, and to adapt the QEC scheme accordingly to take advantage of this noise. This strategy works best when the error structure is preserved as much as possible throughout all gates and measurements.

Stabilized cat qubits are an example of this model[15–20], in which bit flips can be greatly suppressed relative to phase flips then allows us to concatenate these physical qubits with a repetition[18] or thin rectangular surface code[8,21–24] for a substantially improved QEC encoding rate.

A second way to realize this model is with erasure qubits, in which most of the errors can be detected as they occur at the hardware level[10]. After resetting these faulty qubits, the resulting error channel resembles a Pauli error at known spacetime location—an erasure error. QEC codes are generally more tolerant to erasures and can generally correct for twice as many erasures as Pauli errors at a given code distance[5]. They also possess higher thresholds as demonstrated by the surface code, which has a threshold close to 25% for phenomenological erasure noise[12,13].

Erasure qubits are most often realized by detecting loss events that take us out of the computational subspace. For dual-rail qubits, such as those in photonic[25–28] or superconducting platforms, this is loss of a photon or excitation that takes us to the vacuum state. In other platforms, such as neutral atoms or trapped ions, leakage to non-computational states or loss of the atom from the trap can also be detected and converted to an erasure[10,29,30], with similar benefits[9,31].

In superconducting circuit platforms, dual-rail qubits can be realized with pairs of transmons[6,32–34] or microwave cavities[7,35,36]. When idling, dual-rail cavity qubits exhibit a strong hierarchy of errors that make them a promising erasure qubit. In this hierarchy, erasures dominate by a factor of 5–10 compared with phase flips, whereas the remaining bit flips are exceedingly rare. So far, superconducting dual-rail cavity qubits have demonstrated fast, high-fidelity single-qubit gates[37,38], good state preparation and measurement (SPAM)[36], and efficient, non-destructive detection of erasures[39,40]. However, a vital missing ingredient is an entangling operation between two dual-rail qubits, which must simultaneously have low error rates and preserve the favourable error hierarchy.

Here, we propose and experimentally demonstrate a controlled-Z (CZ) operation that satisfies these requirements for dual-rail cavity qubits. Our so-called 'Swap–Wait–Swap' (SWS) gate uses high-fidelity parametric operations to temporarily swap an excitation from one of the cavities (that comprise the dual-rail 'control' qubit) to a transmon coupler connecting the two dual-rail qubits, similar to the scheme in ref. 41. By temporarily populating the coupler, we are able to use the strong (MHz level) dispersive shift between the coupler and a cavity of the other ('target') dual-rail qubit. Swapping the excitation back into the control cavity completes the gate, allowing us to realize a CZ entangling gate in about 500 ns.

Importantly, our gate is bias-preserving in several aspects. The excitation-preserving nature of the gate preserves the erasure-to-Pauli noise bias on both qubits, with erasure rates below 1%. After erasure

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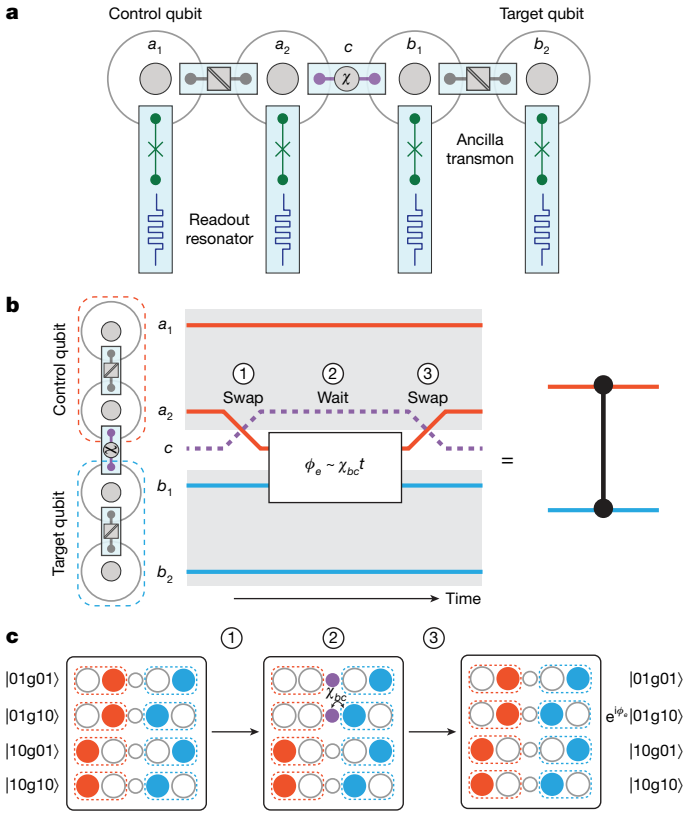

Fig. 1 | Device hardware schematic and CZ gate sequence. a, Schematic of a two dual-rail cavity qubit system, similar to ref. 36, in which the control and target qubits are realized using pairs of three-dimensional $\lambda/4$ coaxial microwave cavities (red and blue). Three SQUID transmon couplers (grey and purple) each dispersively couple to pairs of cavity modes. These couplers are flux-pumped[38] to actuate parametric beamsplitter interactions for single-qubit gates within the dual-rails, and also to implement the dual-rail two-qubit gate, which is achieved by the middle coupler. Each cavity is coupled to an additional transmon qubit (green) and readout resonator (blue lines) that are used for SPAM. **b**, Diagram of the SWS gate sequence between two dual-rail cavity qubits. This gate consists of three steps: (1) performing a Swap operation between the control qubit (a_2 cavity) and the coupler c; (2) allowing the dispersive interaction between coupler and target qubit (b_1 cavity) to acquire phase and entangle the two dual-rail qubits; and (3) effectively switching off this dispersive interaction by performing another Swap between control qubit (a_2 cavity) and coupler, restoring population to the a_2 cavity. **c**, Schematic of photon population during the gate sequence for the four basis states.

detection, we find the residual dephasing errors are at or below 0.1% per gate, as characterized by quantum state tomography (QST) and interleaved randomized benchmarking (IRB). Moreover, we also observe a strong Pauli noise bias in our gate with bit-flip errors at the order of 10^{-6} per CZ gate, an advantageous bias first explored theoretically in ref. 11. Moreover, target qubit erasures and dephasing rates are a factor of 3–4 times lower than those for the control qubit. This asymmetry can be carefully managed when detecting error syndromes in a QEC context (J.D.T., manuscript in preparation) to ensure errors on data qubits are minimized. Finally, we study the error channel when one of the qubits suffers from photon loss during or before the gate, and show both theoretically and experimentally that this amounts to a conditional-dephasing error on the other qubit. All of these properties can be exploited by properly designed error correction codes, as we show with simulations in the surface code (Methods). The performance levels we demonstrate are well past the predicted surface code thresholds obtained from simulations[10] (J.D.T., manuscript in preparation) and should thus allow significant logical error suppression with increasing code distance.

The SWS CZ gate

Our two-qubit gate makes use of a dispersive interaction to implement a CZ gate between two dual-rail qubits, each comprising a pair of nominally linear microwave cavities. For dual-rail cavity qubits, enacting a CZ gate in the Fock basis between two cavity modes (one from each dual-rail qubit) also enacts a CZ gate in the dual-rail basis.

Thus, nearest-neighbour coupling of the cavities is sufficient to implement a dual-rail CZ gate. The physical system shown in Fig. 1a realizes this by using a coupler c to enact a CZ gate on the adjacent a_2 and b_1 cavities. The dispersive interaction we use for this purpose acts between the coupler and cavity mode b_1 in the target qubit, $\mathcal{H}_{\text{int}}/h = ?_{bc}\hat{b}_1^{\dagger}\hat{b}_1\hat{c}^{\dagger}\hat{c}$, where $\chi_{bc}/2\pi = -1.51$ MHz in our system.

Normally, this static interaction term does not affect the system dynamics in any way, and is effectively 'switched off' since the coupler mode c is in its ground state. The interaction can be effectively switched on by attempting to swap a photon between the cavity a_2 and coupler c, temporarily redefining the control dual-rail qubit between the non-local elements a_1 and c (Fig. 1b). Such a swap here is implemented using a parametric sideband interaction between the coupler and cavity: $\mathcal{H}/\hbar = \frac{g_{ac}}{2}(\hat{a}_2^{\dagger}\hat{c} + \hat{a}_2\hat{c}^{\dagger})$, similar to the interaction used to affect single-qubit gates in dual-rails[38]. In our hardware, $g_{ac}/2\pi = 4.23$ MHz. The dispersive interaction is then allowed to act for a time $t \approx \pi/\chi_{bc}$, thus entangling the two qubits. A final swap between the coupler and cavity a_2 returns the excitation back to the control cavity. The entangling phase $\phi_e = \chi_{bc}t_{\text{wait}}$ has thus been imparted only to the $|0,1,1,0\rangle$ initial basis state (using the notation $|a_1,a_2,b_1,b_2\rangle$), which results in a control-phase gate with phase set by the wait time. We adjust this wait time to realize a CZ gate.

Our gate construction allows us to effectively realize a large 'switchable' dispersive interaction between cavity modes a_2 and b_1, without needing to modulate the strength of the underlying static dispersive interactions in our system, which often requires complex Hamiltonian engineering[42]. From this construction, we also expect our gate to exhibit highly structured noise, which is advantageous for QEC syndrome extraction circuits (see the Methods for an example with the surface code and J.D.T., manuscript in preparation).

We now describe this noise structure in detail. The first observation we make is that the total number of excitations are preserved throughout the entire operation. Both control and target dual-rails never leave the single-excitation manifold (redefining the control dual-rail as modes a_1 and c during the gate). This property ensures that any photon loss, even in the coupler mode, leads to a loss error that can be detected after our CZ gate. As an added benefit, we also avoid detrimental effects due to cavity self-Kerr, as no mode is populated with more than one photon at any point during the gate. A caveat, however, is that errors on the target and control qubits can have significant asymmetry. The control qubit, which partially occupies the coupler mode during the gate, experiences increased loss (with probability $t/T_1 \approx 1\%$) and dephasing ($t/T_\phi \approx 0.1\%$) compared with the target qubit ($t/T_{1,\text{cav}} \approx 0.1\%$, $t/T_{\phi,\text{DR}} \approx 0.01\%$), owing to the lower coherence times of the coupler mode compared with the cavities. We term this property of our gate as an error asymmetry. Another property that arises naturally is the strong suppression of bit-flip errors, as observed in the idling state of the dual-rails[36]. This is because the outer cavities a_1 and b_2 and their couplers remain completely idle during the gate. As such, our gate is bias-preserving to dephasing errors. Finally, we expect well-behaved propagation of leakage errors. The dominant leakage channel is decay to the vacuum state, which switches off the CZ-generating cross-Kerr interaction. Thus, if either of the dual-rails relaxes to vacuum, subsequent CZ gates simply do not occur, as if they were omitted from the quantum circuit.

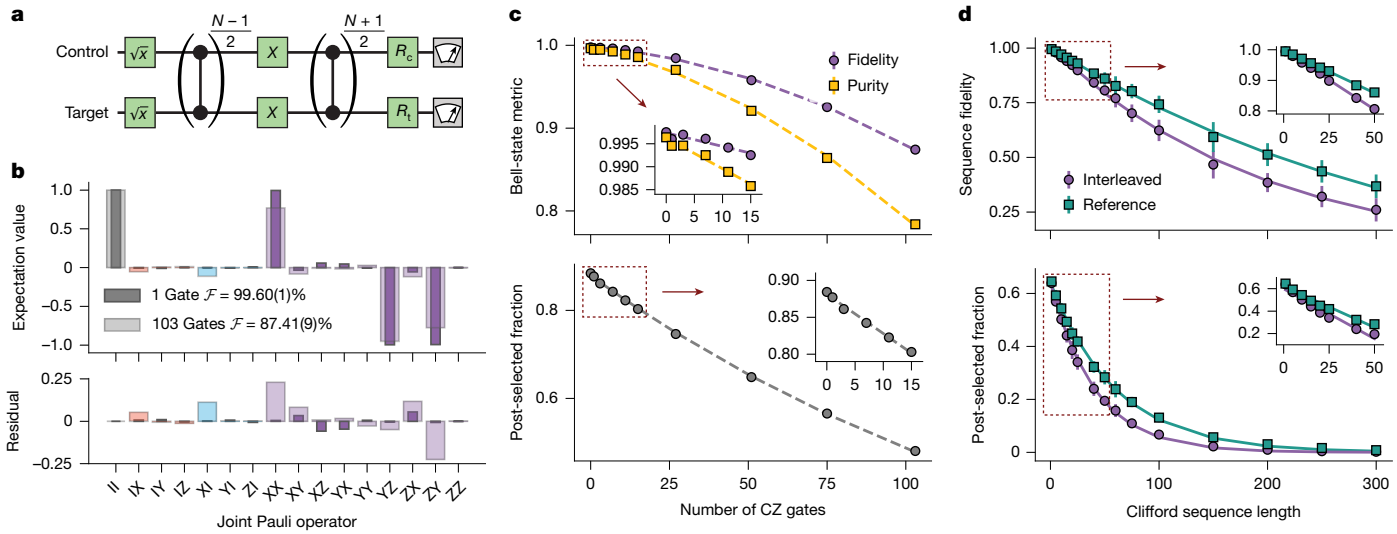

Fig. 2 | Benchmarking a dual-rail qubit CZ gate. a, Gate sequence used to quantify CZ gate fidelity by QST. Applying an odd number N of repeated CZ gates ideally generates a Bell state. For all cases except $N = 1$, X gates are applied to each qubit midway through the sequence, after the first $(N-1)/2$ CZ gates. This serves to echo out low-frequency dephasing noise and to eliminate effects of no-jump-back action (Supplementary Information section VII). By changing the single-qubit gates, R_c and R_t (using an overcomplete gateset spanning $\{I, X_{\pm\frac{\pi}{2}}, Y_{\pm\frac{\pi}{2}}, X_{\pi}\}$), we can extract all 16 joint Pauli correlators for the final state. **b**, QST after applying the gate sequence for $N = 1$ CZ gates (dark) and $N = 103$ CZ gates (light), represented by joint Pauli correlations. The ideal Bell state is defined by $\langle II\rangle = \langle XX\rangle = 1$ and $\langle YZ\rangle = \langle ZY\rangle = -1$, with the residuals shown below. **c**, Repeated CZ gate Bell state tomography showing the increase in gate error with increasing gate repeats. We measure Bell state fidelity (top, purple circles), state purity (top, yellow squares), and post-selected fraction, the fraction of shots for which no erasure errors are detected (bottom, grey), as a function of the number of CZ gates. The insets show data up to $N = 15$ CZ gates. Each tomography setting is averaged 10^6 times. Error bars are generated from bootstrapped resampling of the data and are smaller than the size of the markers. **d**, Two-qubit IRB showing reference (blue squares) and interleaved (purple circles) experiments. Each Clifford sequence, generated from the gateset $\{X_{\frac{\pi}{2}}, Z_{\pm\frac{\pi}{2}}, \mathrm{CZ}\}$, is randomized 20 times and averaged 40,000 times, and the mean and standard deviation over random seeds are plotted. The fraction of shots measured in the two-qubit codespace is plotted in the bottom panel.

Our experimental two-qubit system also exhibits high-fidelity SPAM and single-qubit gate fidelities that aid in the detailed characterization of our two-qubit gate. Single-qubit gates are performed by driving a beamsplitter interaction within the dual-rail for durations of about 200 ns, achieving erasure rates of approximately 0.1% and post-selected randomized benchmarking error of about 0.01%. By using end-of-the-line erasure-detected measurements[36], we are able to obtain low post-selected SPAM errors of about 0.02%. We provide additional results in Supplementary Information section I. A detailed explanation of these parameters and the calibration protocol can be found in Supplementary Information sections II and XIII.

Gate benchmarking

We now present several methods for characterizing the fidelity and error structure of the SWS gate. As with all operations on erasure qubits, we must carefully quantify both the erasure rate and the residual Pauli errors. We use the SWS gate to generate an entangled Bell state, which we analyse using QST. We also perform IRB to evaluate gate performance in arbitrary circuits.

For our first demonstration of the SWS operation, we show high-fidelity entanglement between two dual-rail qubits by implementing the circuit in Fig. 2a with a single CZ gate ($N = 1$). As shown in Fig. 2, we generate a high-fidelity Bell state and, after post-selection of erasures, extract an end-to-end circuit state fidelity of 99.60(1)% and a state purity of 99.46(3)%. We highlight that this infidelity of about 0.4% includes errors aggregated from SPAM, single-qubit gates and the CZ gate.

Next, we perform repeated CZ gates that repeatedly entangle and disentangle the two qubits up to $N = 103$ to establish a more precise metric for the error per CZ gate, using the sequence shown in Fig. 2a. The dependence on the number of gates is shown in Fig. 2c, in which we present state fidelity, state purity and post-selected fraction as a function of the number of repeated CZ gates. First, we can consider the behaviour at lower gate repeats. As shown in Fig. 2c (inset), our data show a linear decrease in fidelity and purity out to $N = 15$ repeated gates, from which we extract a post-selected infidelity of 0.029(6)% per gate.

We also analyse the results for larger gate depths up to $N = 103$. First, we extract the post-selected fraction (Fig. 2c, bottom), defined to be the fraction of experimental shots for which no erasures were detected. From fitting the results to an exponential decay, we extract a total erasure probability per CZ gate of 0.53(2)%. As the number of gates increases, both the fidelity and purity of the final state (Fig. 2c, top) exhibit an unexpected approximately quadratic decrease. We propose the cause to be drift in calibration parameters or fluctuations in the frequency of the coupling transmon on timescales of experimental shot averaging. Our results indicate that dynamical decoupling by adding more X gates between CZ gates does not alleviate this effect. Understanding the root cause of this effect will require further investigation. As a conservative bound for the gate error, we consider the error at $N = 103$ and show the corresponding QST results in Fig. 2b and extract an end-to-end circuit state fidelity of 87.5(1)% and state purity of 78.4(2)%. From this, we infer a bound of 0.12(1)% error per CZ gate, which is among the best reported for superconducting qubits.

As an alternative method for determining the post-selected gate fidelity, we perform IRB to test our CZ gate (Fig. 2d). Because of the finite erasure probability of 0.69(2)% per gate, the usable sequence depth is limited to only a few hundred gates (Fig. 2d, bottom). This complicates the fitting to the typical exponential form expected for sequence yield (Fig. 2d, top). A detailed analysis of gate error extraction can be found in Supplementary Information section IV. We, therefore, use a linear fit at shorter gate depths (Fig. 2d, inset), obtaining an estimate for the error per CZ gate of 0.108(5)% in reasonable agreement with the result from repeated Bell state tomography. See Supplementary Information section V for an analysis on nuanced effects of leakage and seepage errors

(leakage states silently re-entering codespace)[43,44]. In Supplementary Information section XII, we performed repeated IRB benchmarking for up to 15 h on seven different two-qubit systems, with similar properties to the one characterized here.

CZ gate noise structure

Having benchmarked the performance of the CZ gate, we now investigate the structure of gate errors on the control and target qubit and show we preserve the error hierarchy when performing CZ gates. In the following, we measure the error asymmetry for leakage, dephasing and bit-flip errors.

First, we characterize the fraction of detected leakages for our repeated gate Bell state tomography, extracting assigned erasures for the control qubit only, target qubit only, and both qubits, shown in Fig. 3a. As expected, we observe a higher fraction of erasures on the control qubit compared with the target qubit, extracting 0.400(4)% and 0.096(4)% per CZ gate for control and target qubit, respectively. Taken together, this erasure asymmetry of about 4 is consistent with the relative T_1 between the coupler and the average T_1 of the target qubit cavities.

Next, we study the relative fraction of dephasing errors on the control and target qubit. Analysing the reconstructed quantum state from our Bell state tomography, we extract Z errors on the target and control qubit individually as well as correlated ZZ dephasing on both qubits. Our results are shown in Fig. 3b, showing a clear asymmetry in Z errors between the control and target qubit, and small ZZ errors that affect both qubits. From these results, we extract target qubit Z errors of 0.0112(9)% per CZ gate. The control qubit Z errors, however, show the same type of nonlinear behaviour observed for the QST results, suggesting that the root cause of this behaviour could be attributed to some characteristic of the coupler. To quantify the control qubit error, we evaluate at $N = 27$ gate repeats and extract an averaged Z-error of 0.039(1)% per CZ gate. Using the same analysis, we extract ZZ errors of 0.007(1)% per CZ gate. Overall, we observe a dephasing ratio of about 3.5, which is consistent with what we expect from coupler and dual-rail T_ϕ dephasing times. Detailed simulations of the CZ gate error structure can be found in Supplementary Information section XIV.

Idle dual-rail cavity qubits exhibit extremely low bit-flip errors[36], because they require the loss of a photon in one cavity and the gain of a photon in the other (a double error). We expect our CZ gate to also exhibit this property and experimentally confirm only a small increase in bit-flip errors when executing the CZ gate, relative to the idle case, as shown in Fig. 3d. We also further characterize bit-flips on the control and target qubits separately, as summarized in Fig. 3e and Supplementary Information section XI. The total probability of any bit-flip is bounded at a few parts per million per gate, which is probably not limited by 'true' bit-flip errors but rather a photon loss event followed by misassigning a leakage error as being in the codespace in the final. Once again, the asymmetry in observed bit-flips on the control and target qubits is in line with what we expect from the lower T_1 of the coupler.

CZ leakage propagation

Finally, we investigate how the dominant $|00\rangle$ leakage propagates through the CZ gate while awaiting detection by erasure check measurements. Leakage is typically considered to be a particularly damaging error in a QEC context. If not properly controlled, leakage may propagate without bound, resulting in correlated errors and diminished effective code distance.

In our system, we consider two possible leakage scenarios: photon loss to $|00\rangle$, which occurs before a CZ gate and leakage that occurs midway through the CZ gate at an unknown time. We study the more likely scenario of leakage affecting only the control qubit, although due to the symmetry of a CZ gate, our results are expected to apply similarly to the case of leakage on the target qubit. Although other dual-rail leakage states are possible due to cavity heating, such as $|02\rangle$ or $|11\rangle$, these occur at least 1,000 times less frequently in our hardware and are not considered here.

We can first consider what happens if the control qubit is in the $|00\rangle$ state before the CZ gate. As there is only one excitation in the system (in the target qubit), the dispersive interaction does not affect any system dynamics, resulting in an identity operation on the target qubit. The exact same scenario occurs if the control qubit begins in $|10\rangle$ and suffers from photon loss in mode a_1 during the CZ gate: as no photons were ever swapped into the coupler, the dispersive interaction was never activated, which again results in an identity operation on the target.

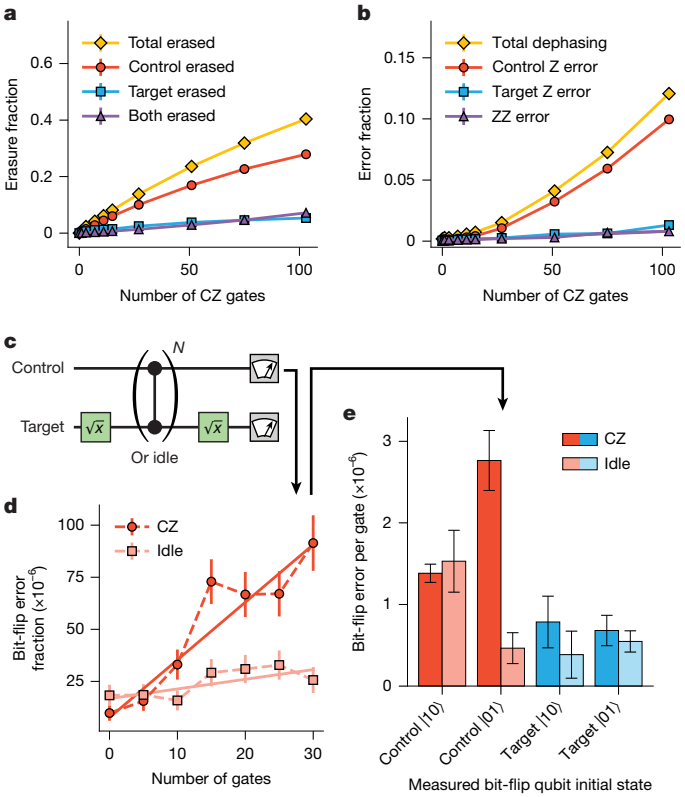

Fig. 3 | Quantifying CZ error structure. a, Extracted erasure fraction. **b**, Z-error fraction after applying a variable number of CZ gates, showing a breakdown for the following categories of dephasing errors: control only (red circles), target only (blue squares), both control and target (purple triangles) and total error (yellow diamonds). For both results, a strong asymmetry between the control and target erasures is observed. Error bars are generated from bootstrapped resampling of the data and are smaller than the size of the markers. **c**, Example circuit to measure control qubit bit-flip errors using a Ramsey-like sequence with a series of N CZ gates or an equivalent delay. The control (target) qubit is initialized in either $|01\rangle$ or $|10\rangle$ to avoid having dephasing errors that could convert into bit-flip errors. Unlike the QST circuit, this experiment is performed without an echo pulse to eliminate a source of extraneous bit-flip errors from the single-qubit gate. **d**, Measured control qubit bit-flip fraction when initialized in $|01\rangle$ as a function of the number of applied CZ gates (circles) and as a function of the equivalent idle (squares). From a linear fit to the data, we infer a total bit-flip error per CZ gate of $2.8(4) \times 10^{-6}$ and $0.5(2) \times 10^{-6}$ when simply idling. Error bars are 95% confidence intervals generated using the Clopper–Pearson method. **e**, Extracted bit-flip error fractions per CZ gate for the control qubit (red, left) and target qubit (blue, right). CZ bit-flip errors are compared against idling errors, showing low bit-flip errors at the level of about 10^{-6} per gate. Each measurement setting is averaged 10^6 times.

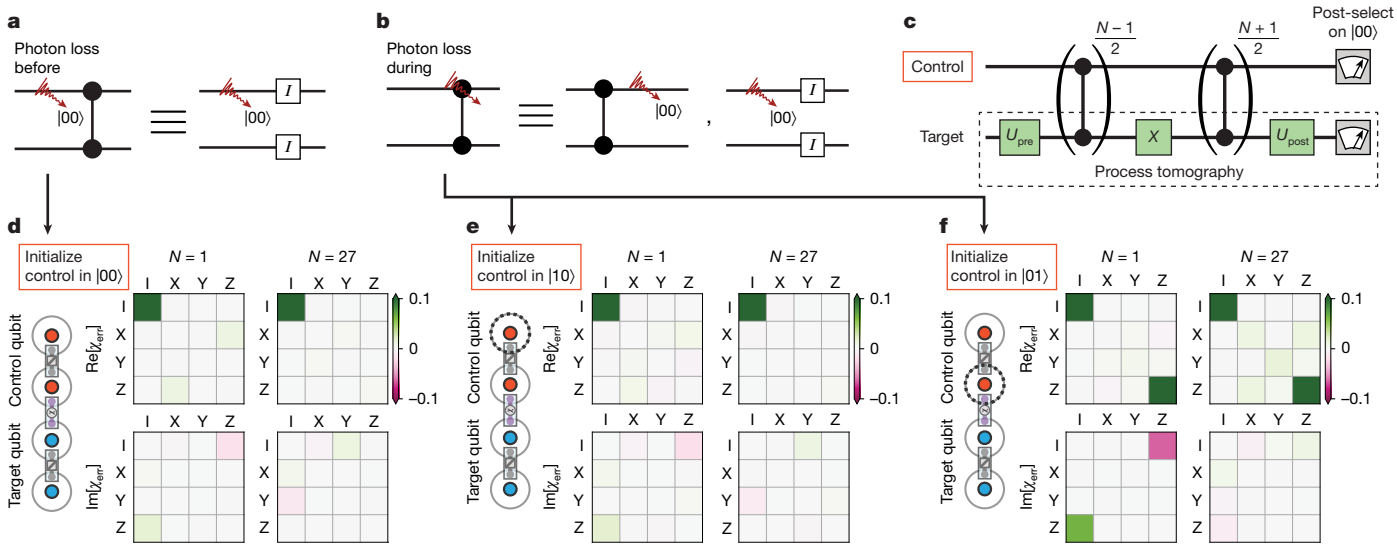

Fig. 4 | Leakage propagation properties of the CZ gate. a, Leakage on the control qubit to |00⟩ before the CZ gate causes the gate to be switched off, and instead the identity process is performed on both qubits. **b**, If photon loss occurs during the gate, the error channel can be accurately modelled as a mixture of leakage occurring before the gate, or after the gate, resulting in what we term a 'CZ error'. **c**, Circuit diagram used to test the leakage propagation properties of the CZ gate. For different preparations on the control qubit, quantum process tomography is performed on the target qubit after applying N CZ gates on the target qubit. To test for control qubit leakage properties, the tomography is conditioned on the control qubit being found in the leakage |00⟩ state. **d**–**f**, Conditioned process tomography on target qubit when the control qubit is prepared in |00⟩, |10⟩ and |01⟩, respectively. To quantify the error channel, we plot the leakage-conditioned quantum process tomography using the χ-error matrix[46] against a reference process, here, the identity channel (Supplementary Information section VI). For each case, the real (top) and imaginary (bottom) part of the χ-error matrices are plotted for $N = 1$ CZ gates (left) and $N = 27$ CZ gates (right). The colour scale is clipped to have a maximum value of 0.1, to make deviations from the expected error channel more visually apparent in the plots. For control qubit initialized in |00⟩ and |10⟩, the expected identity process is observed, indicating that a leakage error turns off the gate; while a dephasing-like error is observed on the target qubit when the control qubit is initialized in |01⟩ indicated by II and ZZ components in the real part of χ-error matrix. This error channel is discussed in detail in Supplementary Information section VI, along with the significance of the IZ and ZI components in the imaginary part of the χ-error matrix. Quantum process tomography is averaged over 10,000 repetitions when starting in |00> and 100,000 times when starting in |01> and |10> states.

The case when the control qubit begins in |01⟩ and swaps into the coupler is more involved. Should excitation loss occur at any time during the gate, the end result is equivalent to performing a CPHASE gate with an unknown rotation angle, and the control qubit ending in vacuum. Averaging over all possible loss times results in what we term a 'CZ error', a correlated error in which the target qubit dephases, but only if the control leaks from the initial |01⟩ state.

This type of 'benign' leakage propagation can be incredibly useful for QEC, by enabling fewer and delayed erasure checks. For instance, in the surface code, we may perform all erasure checks at the end of a round of syndrome extraction rather than after every two-qubit gate (Methods), without significant loss of threshold or effective code distance. A more detailed and theoretical treatment of this leakage error model can be found in Supplementary Information section VI.

We use quantum process tomography to verify and measure these leakage properties, as shown in Fig. 4c. We prepare the control qubit in the known states |01⟩, |10⟩ and |00⟩ and perform N repeated CZ gates followed by process tomography on just the target qubit. In all cases, we require the control qubit to end in the state |00⟩ and post-select accordingly. Our results (Fig. 4d,e for $N = 1$ and $N = 27$ CZ gates) show the expected trivial behaviour when the control qubit begins in |00⟩ or |10⟩ state, and at $N = 1$, we measure the deviation from the ideal identity channel to be Pauli errors on the target qubit with strength 0.19(2)% and 0.18(2)%, when preparing |00⟩ or |10⟩ in the control qubit, respectively. Repeating the gate many times allows us to reduce the contribution from SPAM errors. At $N = 27$, we estimate the fraction of CZ erasures to be roughly two-thirds of total erasures, and measure the target qubit Pauli errors to be 0.012(1)% and 0.013(1)%, respectively, per CZ gate.

Finally, tomography for when the control qubit begins in |01⟩ is shown in Fig. 4f. Visually, the process matrix on the target qubit closely matches a pure dephasing channel. More quantitatively, we extract the deviation from the pure dephasing channel: for $N = 1$ gates, the extracted residual X and Y errors total 0.7(1)%. Similarly, at $N = 27$, we determine this error to be 0.094(2)% per CZ gate. This can be interpreted as an upper bound on the X and Y Pauli errors on the target when the control qubit leaks from |01⟩ during the gate.

Table 1 | Error hierarchy and asymmetry for the SWS gate

Error hierarchy	Total cost per CZ gate	Error asymmetry (control:target)		Error propagation for QEC
		Typical	Measured	
Erasure	$\pi/(\chi_{bc}\, T_1^c) \sim 0.5\%$	10:1	4:1	Z-error on unleaked qubit
Dephasing	$\pi/(\chi_{bc}\, T_\phi^c) \sim 0.1\%$	10:1	3.5:1	Commutes with gate; ancilla dephasing becomes stabilizer measurement error
Bit-flip	$\lesssim 10^{-6}$	10:1	immeasurable	Very rare, contributes to circuit-level depolarizing noise

Values reflect both the typical and measured performance expected for a SWS gate and their effect on QEC schemes.

Discussion and conclusion

The addition of a fast and high-fidelity entangling operation completes the toolbox of gates and operations for dual-rail cavity qubits[7]. We have

experimentally confirmed several properties important for erasure qubits. It preserves (Table 1) the desirable error hierarchy by exhibiting both a strong erasure-to-Pauli noise bias and a dephasing-to-bit-flip noise bias. Furthermore, we observe a significant asymmetry in the errors induced on the control compared with the target qubit. Finally, the gate has a simple error channel in the event that one of the qubit is erased before or during the gate, which is useful for delaying erasure checks in QEC contexts.

Our results present numerous opportunities for operating dual-rail cavity qubits at scale with high-performance: from enabling high-circuit performance for short-depth circuits, to new types of error mitigation through flagging erasures, to—perhaps most excitingly—a viable path for implementing QEC using erasure qubits. As a preview for how well we expect our dual-rail cavity qubits to perform for QEC, in the Methods, we present some preliminary results simulating the performance of a surface code implemented using dual-rail cavity qubits with a more comprehensive treatment in an upcoming publication (J.D.T., manuscript in preparation). We find that even with current CZ gate performance, the error rates are already a factor of ten below the respective erasure and dephasing thresholds. Further improvements in physical error rates can also be straightforwardly achieved through improvements in beamsplitter rates to increase gate speed and through improving the coherences of, primarily, the coupler. In the presence of both kinds of errors, detailed numerical simulations (J.D.T., manuscript in preparation) are needed to estimate the actual performance, but the results described here provide a path to realize large error correction gains of 10 or more with an increase in code distance in the near future. All of these results highlight that superconducting dual-rail cavity qubits have quickly become an attractive path for achieving fault-tolerant quantum computing. During the completion of this paper, we became aware of related work on implementing the two-qubit gates using tunable dual-rail transmon qubits[45].

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-026-10822-y.

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Methods

Quantum error correction benefits of structured noise in our CZ gate

Our SWS gate possesses an error structure that can be leveraged to reduce errors during syndrome extraction in stabilizer codes such as the surface code. Here, we show simulations using Stim[47] that support and quantify this claim by studying the reduction in logical error rate compared with code distance in a surface code memory. More complete simulations results and methodology will be the subject of an upcoming, separate publication (J.D.T., manuscript in preparation), which solely focuses on QEC scaling in a dual-rail cavity qubit surface code.

There are four aspects to the SWS gate error structure that are expected to improve syndrome extraction circuits in general:

- Erasures (leakages to $|00\rangle$) occur much more frequently than Pauli errors.
- Pauli errors are mostly dephasing errors; bit flips are rare.
- We can designate the 'control' qubit to be the ancilla, which then picks up most of the erasure and dephasing errors, leaving the data qubits mostly error-free.
- Once a qubit has leaked to $|00\rangle$, subsequent CZ gates are skipped, which allows us to perform less frequent erasure checks.

We quantify error correction performance by extracting Λ, the factor by which the logical error rate (per syndrome extraction round) decreases when the surface code distance is increased by 2 (refs. 3,4). We compare two noise models. The first is a noise model in which only the CZ gates are error prone, and the error rates for all CZ gates are identical to the values shown in the paper at low repeated gate depth, that is, ancilla erasure = 0.4%, data erasure = 0.1%, ancilla dephasing = 0.04%, data dephasing = 0.01%, joint dephasing = 0.01%, ancilla bit flip = 0.0003%, data bit flip = 0.00005%. We also include perfect erasure checks, which are delayed to the end of the syndrome extraction round (see next section in Methods as to why we make this choice). The second noise model uses only a two-qubit depolarizing noise channel after each CZ gate as the only source of error, a well-studied noise model with a threshold close to 1%. For this noise model, we set the error rate $p = 0.1\%$ to reflect state-of-the-art performance in other two-qubit gates with 'unstructured' errors. Both simulations to extract Λ are performed using Stim. For the first error model, leakage errors cause subsequent CZ gates to be omitted from the simulation (a property confirmed experimentally in Fig. 4), until the qubit is detected and reset, which is crucial for accurately modelling the propagation of leakage errors with delayed erasure checks. The results shown in Extended Data Fig. 1 show $\Lambda \approx 14$ for the depolarizing noise model and $\Lambda \approx 27$ for our SWS gate error model, demonstrating the benefits of structured errors. More detailed analysis can be found in our upcoming publication (J.D.T., manuscript in preparation). We reiterate that these noise models are chosen to be simplistic, to allow direct comparison between the two-qubit gate errors. More realistic simulations must include errors in the single-qubit gates, all measurements (including erasure checks) and idling errors, which reduce the value of Λ.

Leakage propagation and delayed erasure checks in a dual-rail surface code

A key property of our SWS gate is that attempting to perform the gate when one of the qubits has leaked to $|00\rangle$ before the gate results in identity being performed on both qubits, and excitation loss at any point in time during the gate can be accurately modelled as a CPHASE gate of unknown angle (between 0 and π) followed by photon loss on one of the dual-rail qubits. These properties were experimentally verified in Fig. 4. Here, we show with simulations that this property can be leveraged to delay all mid-circuit erasure checks to the end of the syndrome extraction round, without significant loss of code distance or threshold we expect from erasure qubits.

Performing erasure checks once every four CZ gates (rather than after every CZ gate) makes us much less prone to errors in the erasure checks themselves, which is vital for achieving good error correction performance in practice. This also, in principle, enables us to avoid mid-circuit erasure detection entirely in a surface code, by instead detecting erasures by 1-bit Knill-style teleportation in between syndrome extraction rounds[48] (that is, teleporting back and forth between data and ancilla qubits, and performing a 'destructive' erasure check whenever a qubit is measured out in an end-of-the-line measurement). As such, the importance of a high-fidelity, fast mid-circuit erasure check may have been previously overemphasized for erasure qubitsthat possess this 'leakage skips subsequent gates' property.

To verify these claims, we perform Stim simulations in which the data qubit and ancilla qubit each have probability $p/2$ of leaking to the $|00\rangle$ state after every CZ gate, and subsequent CZ gates are skipped (that is, omitted from the quantum circuit) if any one of the qubits in the CZ pair are in $|00\rangle$. We then perform perfect erasure checks at the end of each round. From Extended Data Fig. 2, we extract a threshold of 5.6% and verify preservation of the effective code distance by fitting the logical error rate to the model $p_L \propto p^{\alpha d}$. We find $\alpha = 0.93$, close to the value of 1 expected for erasure-like errors. For Pauli-like errors, $\alpha = 0.5$ is expected instead.

The threshold we find is slightly higher than that obtained in ref. 10, in which a threshold of 5.13% was obtained for an error model with perfect erasure checks after every CZ gate, but also assumed leakage during a CZ gate caused a depolarizing error on the other qubit, which we believe introduces more entropy (and more possible syndromes to decode) than our error model.

When delaying erasure checks to the end of the syndrome extraction round, there is an increased uncertainty with regard to the exact time location of the leakage event in the syndrome extraction gate sequence. However, we find that this added uncertainty does not lead to any bad hook errors. This property can be verified by exhaustively sampling detector flip patterns for all possible locations of a single leakage event in the previous syndrome extraction round. This lack of hook errors is also thought to be the reason why we obtain α close to 1, preserving the scaling with code distance expected for typical erasures. Delayed erasure checks will be studied more extensively in an upcoming publication (J.D.T., manuscript in preparation).

Data availability

The data that support the findings of this study are available on Zenodo at https://doi.org/10.5281/zenodo.20433754.

Code availability

The code used to generate the QEC simulation results will be presented in an upcoming publication (J.D.T., manuscript in preparation).

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Acknowledgements We thank L. Frunzio, A. Kubica, S. Xue, J. Garmon, and T. Tsunoda for their feedback on the manuscript.

Author contributions J.D.T. and S.O.M. contributed to the proposal and concept of the SWS gate. S.O.M. led the design of the dual-rail hardware architecture. J.O.Y. led hardware deployment, experimental setup and system validation. B.C. led the device fabrication. C.U.L. led the cavity design, preparation and testing. K.S.C. led two-qubit gate testing, measurements and analysis. N.M., T.N., P.L., B.H.E., A. Agrawal, A.N., K.S.C, J.O.Y. and J.D.T. contributed to data acquisition and data analysis. T.N., N.M., P.L., A. Agrawal, K.S.C. and J.D.T. contributed to the SWS gate calibration procedure. J.D.T. and K.S.C. contributed to numerical simulations of the SWS gate. P.L., N.M., J.O.Y., T.N., A. Agrawal, B.H.E., G.L., K.S.C. and N.K. contributed to system bring-up and calibration. S.O.M., R.A.C., S.M.F., T.Z., R.D.L., H.M., D.K.W. and J.O.Y. contributed to quantum hardware design and simulation. E.L., B.B., M.C., C.F. and M.R. contributed to mechanical design. S.O.M. and R.A.C. contributed to coupler design and flux-pump delivery. C.U.L., C.K., J.O.Y., B.H.E., A.S. and N.K. contributed to cavity preparation and testing. J.S., A.B.,

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Funding All authors declare no relevant funding.

Competing interests Authors affiliated with D-Wave Quantum Inc. have financial interest in the company. R.J.S. is a shareholder and consultant for D-Wave Quantum Inc. J.D.T., S.O.M., N.M., K.S.C., T.N., S.H.M. and R.J.S. have filed a provisional patent (application no. PCT/US2025/054681) for the SWS entangling operation.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41586-026-10822-y.

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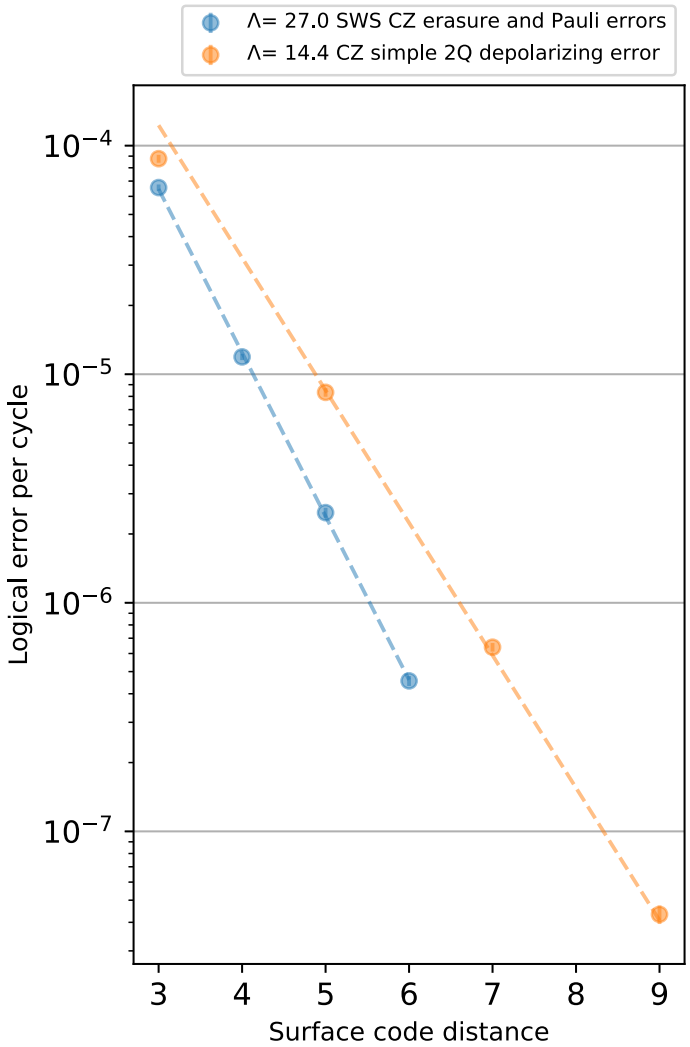
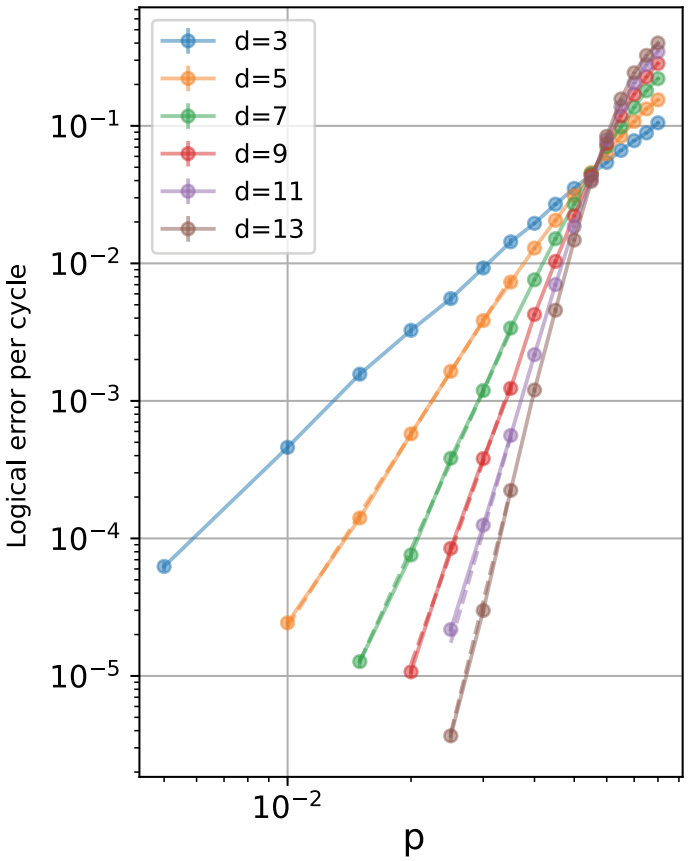
Peer review information *Nature* thanks Pei Zeng and the other, anonymous, reviewer(s) for their contribution to the peer review of this work. Peer reviewer reports are available.



Extended Data Fig. 1 | Simulated surface code memory scaling vs code distance, to compare structured noise in our SWS gate (blue) vs. unstructured CZ gate noise in the form of two-qubit depolarizing noise (orange) with strength 0.1%. Fits to a simple exponential shown with dashed lines are used to extract Λ, the reduction factor in per-cycle logical error rate when the code distance increases by two. For the blue plot, the error rate per CZ gate are chosen to be the same as the values reported in Fig. 3. Having predominantly erasure errors allows us to simulate at even code distance. Despite our total CZ gate error being ~0.5%, around 5 times higher than other state-of-the-art two-qubit gates, we obtain a value of Λ that is roughly double that of simple depolarizing noise. This provides strong evidence that the structured noise in our SWS gate can be leveraged to improve quantum error correction and is on-par with, or better than current state-of-the-art two qubit gates with 0.1% Pauli errors when used in a surface code.



Extended Data Fig. 2 | Simulated surface code memory under erasure errors with delayed, perfect erasure checks. Results are averaged over the X and Z basis, under an error model that includes only erasures in the native CZ gates with total erasure rate p per gate, and perfect erasure checks that are delayed to only occur at the end of each stabilizer round. Dashed lines are fits from which we extract a threshold of 5.6% and $\alpha = 0.93$ (from fitting the function $p_L \propto (p/p^*)^{\alpha d}$ below threshold), showing that delaying erasure checks to the end of each stabilizer round still preserves the favorable error-correction properties of erasures, under our 'leakage skips subsequent gates' error model. Showing these favorable QEC properties in the presence of imperfect erasure checks, and with many other noise sources accounted for is the subject of an upcoming publication (J.D.T., manuscript in preparation).