D-Wave Gate-Model Quantum Computing with Superconducting Dual-Rail Qubits

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Advancing Gate-Model Quantum Computing Through Dual-Rail Architecture

While annealing quantum computing is showing value today for optimization, quantum simulation, and AI, gate-model quantum computers, once commercialized, are expected to be especially powerful for quantum chemistry, materials science, and AI. Gate-model quantum computing remains in the R&D stage today, with error correction serving as a key requirement for fault tolerance and future commercial-scale applications.

D-Wave is developing gate-model quantum systems using a superconducting dual-rail qubit (DRQ) architecture designed to support error detection at the single-qubit level. Because error correction is essential to fault-tolerant gate-model quantum computing, this approach provides what D-Wave believes is a more efficient path to scalable systems. For researchers, it offers a way to investigate error-correction algorithms and post-NISQ applications with greater visibility of when and where errors occur during computation.

Dual-Rail Qubits: The Power of Error Detection

D-Wave's gate-model approach is based on a first-of-its-kind superconducting cavity-based DRQ architecture that embeds error detection directly at the physical hardware level. The technology is designed to deliver high-performance operations with error detection and 99.9%+ gate fidelities, while keeping operations fast.

One persistent challenge with error correction is the large number of additional physical qubits required to protect each logical qubit. In conventional quantum-error-correction approaches, the qubit overhead can drive significant infrastructure, power, and cost requirements. The DRQ is designed to open efficient pathways for error correction, dramatically reducing such overhead, while enabling unique, error-aware programming possible only with D-Wave's tools.

The DRQ's ability to detect errors in real time can inform a user when and where an error occurs at the single-qubit level. This provides critical, actionable information about how to correct errors using fewer qubits. This error-aware capability introduces novel sources of data that can be leveraged for near-term application exploration in regimes that extend beyond what conventional gate-model systems have provided to date, presenting exciting opportunities to discover prototype use cases in preparation for error-corrected dual-rail systems.

The Dual-Rail Qubit Architecture

The DRQ is a composite quantum processing unit (QPU) that uses carefully designed resonators, transmons, couplers, and readout elements to execute gates, detect errors, and perform measurements. As shown in Figure 1, two cavities encode the quantum bit of information in a single, shared photon (yellow disk in Figure 1). The valid computational states are logical "0," logical "1," as in the diagram. The dual-rail qubit also can be put in any arbitrary superposition, and the diagram conveys this through the label "0+1." The DRQ is designed such that the dominant error mode is photon loss. This type of error results in an invalid state that is detectable by the DRQ directly, which raises an error flag. By detecting errors in this way, highly efficient error-correction schemes are possible (see the dotted box in Figure 1). Built using a superconducting cavity-based approach, DRQs are powerful qubits that operate with excellent coherence, support high-fidelity gates, and deliver strong measurement performance.

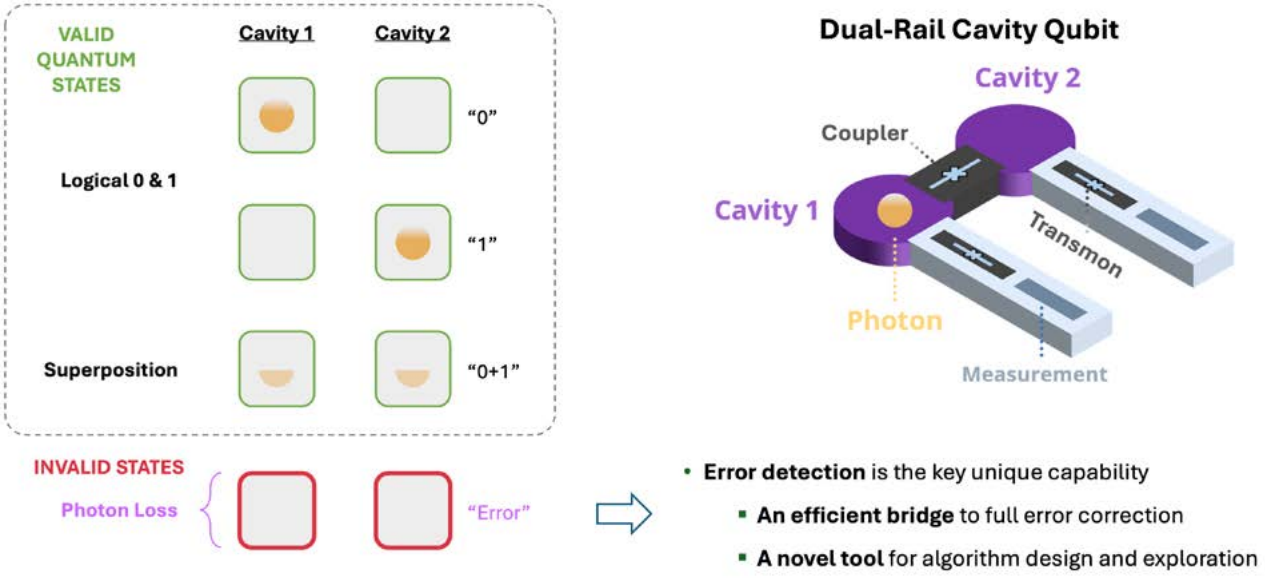

Figure 1 – DRQ and logical encoding

DRQs perform gate operations just as other QPUs in the gate-model industry, with gate operations such as bit flips and entangling gates.

Error-Aware Programming Toolbox

Error-detection capability produces a new type of measurement data, denoted as a star "*," that complements the typical qubit "0" and "1" measurements. These "*" measurements offer novel mechanisms for implementing efficient, advanced error-correction methods, and exploring new quantum-error-mitigation techniques. They enable algorithm development at the intersection of quantum, ML, AI, and more. The error-aware toolbox is depicted in Figure 2.

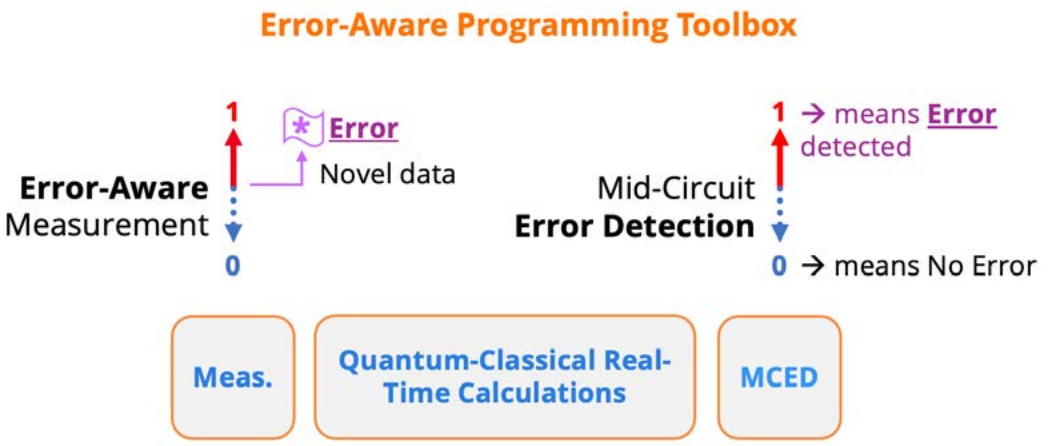

Figure 2 - Error-aware toolbox depicting enhanced programming tools including error detection and real-time control

With these hardware and software capabilities, users and programmers are equipped with three core system features:

- **Error-aware measurement** in hardware, enabled by D-Wave's DRQ error-detection capability. It produces three possible measurement results – 0, 1, and * – where * indicates a measured error.
- **Mid-circuit error detection** (**MCED**) in hardware, enabled by D-Wave's DRQ error-detection capability. It produces two measurement results – 0 and 1 – which indicate whether an error occurred during the execution of an algorithm.
- **Real-time control flow** (**RTCF**) tools to tightly couple quantum-classical programming.

Together, these system capabilities provide two key benefits:

1. **Accelerated path to error correction by reducing the overhead**, or number of qubits needed by a factor of 10, as compared with conventional approaches.
2. **Exploring new classes of algorithms by adding error detection into quantum workflows** for the first time. The ability to detect and respond to errors in real time expands what is possible in algorithm development, creating a foundation for long-term value.

RTCF will be available through the D-Wave™ gate-model quantum simulator and is planned to be rolled out incrementally on quantum systems as the generations of D-Wave's gate-model QPUs continue to grow in capability.

Error-Aware Programming and Simulation

One of the key advantages of DRQs is that, with D-Wave's error-aware tools, users will be able to learn which qubit experienced an error, and when the error occurred in the algorithm in real time. D-Wave will offer a full-stack programming environment supporting hardware-based error detection, run-time control, and error-correction functions. D-Wave will also provide a quantum-computing-as-a-service (QCaaS) ecosystem through its Leap™ cloud platform and Ocean™ SDK. These will be the primary channels of accessing D-Wave's gate-based systems.

Cloud access will be complemented by a feature-rich compiler, a control system that enables RTCF, and Python libraries for programming and software development. D-Wave's Quantum Circuit Description Language (QCDL) API will provide a variety of features that support error-aware programming and simulation at different levels of the stack. For example, in addition to supporting the standard library of universal gate-based operations provided by packages such as Qiskit, QCDL directly surfaces RTCF and error-detection APIs such as the MCED shown in Figure 2. Applications with visibility into quantum-error detection can therefore be written efficiently, opening the door for a new class of integrated quantum and classical algorithm development.

D-Wave is planning to provide two types of quantum simulation capabilities: noiseless and noisy simulators.

- The **noiseless simulator** supports fast algorithm development and prototyping in the absence of errors.
- The **noisy simulator** helps users evaluate how algorithms may perform under more realistic conditions, including with detectable errors.

With the noisy simulator, users will be able to prototype and validate the quantum algorithms and applications using QCDL API before running the code on the QPU.

Beta Access

For users interested in exploring the frontier of fault-tolerant quantum computing, D-Wave will be offering opportunities to engage with its gate-model program including:

- Access to D-Wave's gate-model simulator later in 2026.
- Access to D-Wave's gate-model systems as they become available.
- Access to D-Wave's Leap cloud platform and Ocean SDK.
- Ability to develop a new class of innovative error-aware and error correction quantum algorithms.
- A path toward acquiring a high-performance, error-aware quantum computer, with favorable terms and engineering support.

Explore Error-Aware Gate-Model Quantum Computing

D-Wave develops and supports two leading superconducting technologies: annealing quantum technology and gate-model quantum technology based on the innovative DRQ architecture. Together, these approaches reflect D-Wave's dual-platform strategy and will give customers access to different quantum technologies for different classes of computationally complex problems through a unified ecosystem.

By combining superconducting DRQs with built-in error detection and error-aware programming tools, we believe D-Wave will enable novel applications and support more reliable, scalable gate-model quantum computing as the technology matures.

Request updates on future access to D-Wave's forthcoming simulator or contact sales@dwavesys.com to learn more.